WHAT IS CLAIMED IS:

1. A storage circuit comprising:

a first logic gate for receiving a first signal and a second signal, and for selectively outputting either the first signal or the second signal in accordance with a control signal;

a first storage element for receiving a clock signal, for storing an output signal of the first logic gate in response to the clock signal, and for outputting the stored signal in response to the clock signal; and

a second logic gate for receiving an output signal of the first storage element, and for outputting or fixing the output signal of the first storage element in response to the control signal.

2. A storage circuit according to claim 1, further comprising:

a third logic gate for receiving the output signal of the first storage element, and for outputting or fixing the output signal of the first storage element in response to a complementary signal of the control signal.

3. A storage circuit according to claim 1, wherein

when the control signal is in a first state, the second logic gate outputs the output signal of the first storage element; and

when the control signal is in a second state,

the second logic gate outputs any value of operation voltages of the storage circuit.

4. A semiconductor integrated circuit comprising:

a first storage circuit including first and second input terminals, first and second output terminals, and a first control terminal for receiving a control signal;

a logic circuit for receiving an output signal of the first output terminal of the first storage circuit, for performing a predetermined processing on the output signal, and for outputting a result of the processing; and

a second storage circuit including third and fourth input terminals, and a second control terminal for receiving the control signal, wherein

when the control signal is in a first state, the first storage circuit stores a first signal, which is input to the first input terminal, to output the stored first signal to the first output terminal;

when the control signal is in a second state, the first storage circuit makes a voltage of the first output terminal to be any voltage of the operation voltages of the logic circuit, and stores a second signal, which is input to the second input terminal, to output the stored second signal to the second output terminal;

when the control signal is in the first

state, the second storage circuit stores an output of the logic circuit which is input to the third input terminal; and

when the control signal is in the second state, the second storage circuit stores an output of the second output terminal of the first storage circuit which is input to the fourth input terminal.

5. A semiconductor integrated circuit according to claim 4, wherein

the semiconductor integrated circuit operates by receiving a clock signal; and

the first storage circuit stores the first signal or the second signal at a first timing of the clock signal, and outputs the stored first or second signal at a second timing of the clock signal.

6. A semiconductor integrated circuit according to claim 4, wherein

when the control signal is in the first state, the first storage circuit further makes a voltage of the second output terminal to be any voltage of the operation voltages of the logic circuit.

7. A semiconductor integrated circuit according to claim 4, wherein

when the control signal is in the first state, the semiconductor integrated circuit is in a normal operation mode; and

when the control signal is in the second state, the semiconductor integrated circuit is in a

test mode.

8. A semiconductor integrated circuit according to claim 4, wherein

the first storage circuit and the second storage circuit are scan flipflops.

9. A semiconductor integrated circuit comprising:

a first storage circuit including first and second input terminals, first and second output terminals, and a first control terminal for receiving a control signal;

a first logic circuit for receiving a first output signal of the first output terminal of the first storage circuit, for performing a predetermined first processing on the first output signal, and for outputting of the first output signal;

a second storage circuit including third and fourth input terminals, third and fourth output terminals, and a second control terminal for receiving the control signal;

a second logic circuit for receiving a second output signal of the third output terminal of the second storage circuit, for performing a predetermined second processing on the second output signal, and for outputting of the second output signal; and

a third storage circuit including fifth and sixth input terminals, and a third control terminal for receiving the control signal, wherein

when the control signal is in a first state, the first storage circuit stores a first signal, which is input to the first input terminal, to output the stored first signal to the first output terminal;

when the control signal is in a second state, the first storage circuit stores a second signal, which is input to the second input terminal, to output the stored second signal to the first output terminal;

when the control signal is in the first state, the second storage circuit stores the first output signal, which is input to the third input terminal, to output the stored first output signal to the third output terminal;

when the control signal is in the second state, the second storage circuit makes a voltage of the third output terminal to be any voltage of operation voltages of the second logic circuit, and stores an output from the second output terminal of the first storage circuit, which is input to the fourth input terminal, to output the stored output to the fourth output terminal;

when the control signal is in the first state, the third storage circuit stores the second output signal which is input to the fifth input terminal; and

when the control signal is in the second state, the third storage circuit stores an output from the fourth output terminal of the second storage

circuit which is input to the sixth input terminal.

10. A semiconductor integrated circuit according to claim 9, wherein

when the control signal is in the second state, the first storage circuit further makes a voltage of the first output terminal to be any voltage of operation voltages of the first logic circuit.

11. A semiconductor integrated circuit according to claim 9, wherein

a specification of a delay time of the first logic circuit is shorter than a specification of a delay time of the second logic circuit;

a specification of power consumption of the first logic circuit is set to be smaller than a specification of power consumption of the second logic circuit; and

when the control signal is in the second state, the first storage circuit stores the second signal, which is input to the second input terminal, to outputs the stored second signal to the output terminal.

12. A semiconductor integrated circuit according to claim 9, wherein

a path length from the fourth output terminal to the sixth input terminal is shorter than a path length from the second output terminal to the fourth input terminal; and

when the control signal is in the first

state, the first storage circuit further makes a voltage of the second output terminal to be any voltage of operation voltages of the first logic circuit.

13. A semiconductor integrated circuit according to claim 9, wherein

a specification of a delay time of the first logic circuit is shorter than a specification of a delay time of the second logic circuit; and

a specification of power consumption of the first logic circuit is set to be smaller than a specification of power consumption of the second logic circuit;

a path length from the fourth output terminal to the sixth input terminal is shorter than a path length from the second output terminal to the fourth input terminal;

when the control signal is in the first state, the first storage circuit makes a voltage of the second output terminal to be any voltage of operation voltages of the first logic circuit; and

when the control signal is in the second state, the first storage circuit stores the second signal, which is input to the second input terminal, to outputs the stored second signal to the first output terminal.

14. A semiconductor integrated circuit according to claim 9, wherein

the semiconductor integrated circuit operates

receiving a clock signal; and

the first to third storage circuits store a signal from a circuit of a previous stage at a first timing of the clock signal, to output the stored signal to a circuit at a later stage at a second timing of the clock signal.

15. A semiconductor integrated circuit according to claim 9, wherein

when the control signal is in the first state, the semiconductor integrated circuit is in a normal operation mode; and

when the control signal is in the second state, the semiconductor integrated circuit is in a test mode.

16. A semiconductor integrated circuit according to claim 9, wherein the first to third storage circuits are scan flipflops.